20. (Amended) The DRAM of claim 19, wherein the substrate voltage regulator circuit comprises:

a series of [diodes] diode connected transistors coupled between a supply voltage source and the integrated circuit substrate, and at least one bypass transistor coupled to at least one diode connected transistor in the series of [diodes] diode connected transistors for electrically bypassing the one diode connected transistor.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on August 26, 2002, and the references cited therewith.

Claims 19-20 are amended, no claims are canceled, and no claims are added; as a result, claims 19-43 remain pending in this application.

§112 Rejection of the Claims

Claims 19-43 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 19-43 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The rejections state that, "There is no original disclosure relating to forming an integrated circuit. There is no original disclosure relating to dynamic random access memory (DRAM) or to an array of memory cells." The rejection further states that, "There is no disclosure of what is contained in the charge pump of how it and the other circuitry would form a voltage regulator.

Applicant respectfully traverses the rejection and submits that use of embodiments of Applicant's invention in a memory device are discussed and supported on page 1, lines 8-16. Applicant further submits that one of ordinary skill in the art will recognize that a memory device

includes DRAM's which in turn include an array of memory cells.

Regarding the charge pump, applicant respectfully traverses the rejection and submits that several possible charge pump configurations are included within the scope of the claims, and that configurations of charge pumps are enabled within the skill of one of ordinary skill in the art. Pursuant to MPEP § 2173.04, Applicant notes that "breadth of a claim is not to be equated with indefiniteness."

Regarding the voltage regulator, applicant respectfully traverses the rejection and submits that embodiments as described in the specification and claims "regulate" a "voltage" in a substrate. For example, on page 4, lines 6-9, "The charge pump CP maintains the voltage level of the substrate at that level set by the diode chain. The substrate voltage level is substantially equivalent to the supply voltage Vcc, less any voltage drops across the drain and source of each of the MOSFETs M1, M2, M3, and M5 which are not shorted out of the chain."

Regarding other concerns expressed in the pending Office Action, Vcc is defined as a supply voltage on page 2, line 24. Vbb is defined on page 3, lines 8-10 as being coupled to the substrate. The output of the charge pump is discussed on page 4, lines 5-6.

Reconsideration and withdrawal of the 35 USC § 112, first paragraph rejections is respectfully requested.

Claims 19-43 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claims the subject matter which applicant regards as the invention.

The rejection states that, "it is not clear what the claimed elements are, or how they would function." Applicant respectfully traverses the rejection and submits that the claims are definite under the requirements of 35 U.S.C. 112, second paragraph.

As discussed above, For example, on page 4, lines 7-9, "The substrate voltage level is substantially equivalent to the supply voltage Vcc, less any voltage drops across the drain and source of each of the MOSFETs M1, M2, M3, and M5 which are not shorted out of the chain." In one embodiment, diodes drop a voltage selectively through use of bypass transistors.

Reconsideration and withdrawal of the 35 USC § 112, second paragraph rejection is respectfully requested.

§103 Rejection of the Claims

Claims 19-43 were rejected under 35 USC § 103(a) as being unpatentable over McLaury in view of Bynum et al., Yim et al and Sawamura.

As a preliminary matter, Applicant respectfully requests more detailed references to element numbers and text of the cited documents that the Examiner regards as corresponding to Applicant's claims. Applicant respectfully submits that the level of complexity in the references warrants such detail. Applicant thanks the Examiner in advance for assistance in this matter.

The rejection states that, "McLaury shows apparatus for regulating substrate bias."

McLaury appears to show a diode series 10. The reference also appears to show a diode load element 110. Embodiments of McLaury also appear to show a sense element as part of the integrated circuit. However, Applicant is unable to find at least one **bypass transistor** to at least one diode in a series of diodes for electrically bypassing at least one diode. In contrast, Applicant's independent claims all include at least one bypass transistor coupled to at least one diode in a series of diodes for electrically bypassing at least one diode.

The rejection states that, "Bynum et al shows the concept of controlling the bias applied to a substrate by shunting a diode in a line that applies a voltage to a substrate."

Bynum appear to show an integrated circuit designed to bias an epitaxial well. Embodiments of Bynum appear to include a single diode 42. Bynum also appears to show a shunt path in embodiments using the diode. However, Applicant is unable to find at least one **bypass transistor** to at least one diode in a **series of diodes** for electrically bypassing at least one diode. Applicant respectfully submits that a shunt is not equivalent to a bypass transistor. In contrast, Applicant's independent claims all include at least one bypass transistor to at least one diode in a series of diodes for electrically bypassing at least one diode.

The rejection states that, "Yim et al shows that plural diodes may be used in a line to tailor the applied voltage."

Yim appears to show a voltage drop stage 10 that includes a plurality of MOSFET's whose gates are connected with their drains. However, Yim does not show at least one **bypass transistor** to at least one diode in a series of diodes for electrically bypassing at least one diode. In contrast, Applicant's independent claims all include at least one bypass transistor to at least one diode in a series of diodes for electrically bypassing at least one diode.

Applicant respectfully submits that Sawamura does not cure the deficiencies of the references discussed above.

Because the cited references, either alone or in combination, do not show every element of Applicant's independent claims, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claims 19, 22, 27, 30, 33, 37, and 41. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-373-6944) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

GARY R. GILLIAM

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 25th day of November, 2002.

Name Amy Moriarty

Signature

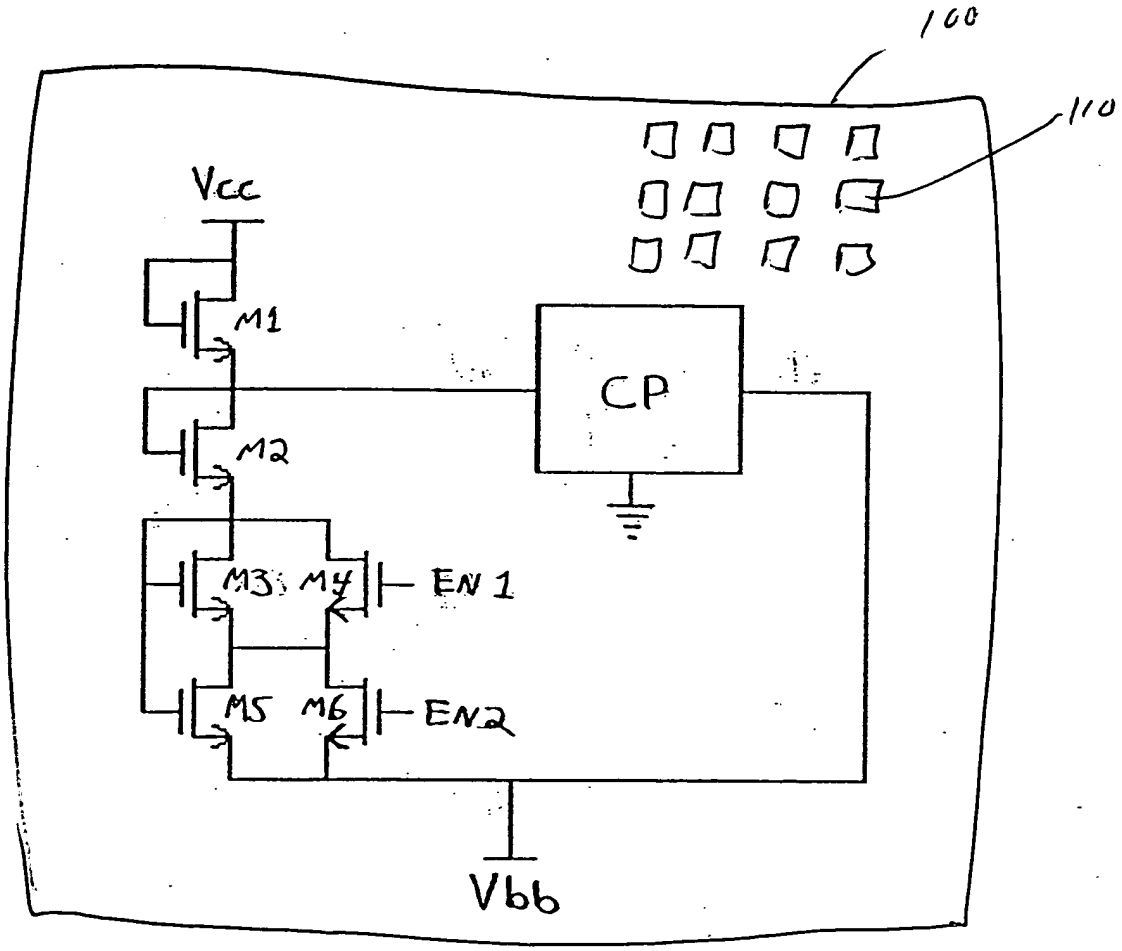

Figure 1